ABSTRACT OF THE DISCLOSURE

A clock data recovery (CDR) circuit to recover a clock signal and data signal from an input signal. The CDR circuit includes a control circuit, a select circuit and a phase adjust circuit. The control circuit generates a first control signal according to a phase relationship between the input signal and a first clock signal. The select circuit is coupled to receive the first control signal from the control circuit and coupled to receive a second control signal. The select circuit is responsive to a select signal to select either the first control signal or the second control signal to be output as a selected control signal. The phase adjust circuit is coupled to receive the selected control signal from the select circuit, the phase adjust circuit being responsive to the selected control signal to adjust the phase of the first clock signal.